

Appl. No. : 09/037,945  
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cont 1  
A1  
4. (Amended) The process of Claim [1, further comprising] 3, wherein forming the field isolation region comprises maintaining the [semiconducting wafer] semiconductor substrate at a temperature greater than 900 °C.

Pub  
B2  
A2  
8. (Amended) A field isolation region among integrated circuit devices on a semiconductor [wafer] substrate formed by a process comprising:

exposing a field region of the semiconductor [wafer] substrate to [an] a dry oxidizing ambient [comprising substantially only oxygen] at a pressure between about 5 atm and 30 atm without a further wet oxidation.

6p  
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6p. (Amended) The field isolation region of Claim 8, wherein the [oxidizing ambient is maintained at a pressure greater than 5 atm and] semiconductor substrate is maintained at a temperature greater than 900 °C while exposing the field region.

Please add the following claims:

Pub  
B3  
A3  
11. (Newly Added) A process of forming electrically isolated integrated devices in a silicon substrate, comprising:

masking portions of the substrate to define unmasked field isolation regions;  
growing field oxide in the field isolation regions by dry oxidation alone at an oxidant partial pressure of greater than about 5 atm and a temperature of greater than about 900°C; and

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forming electrical devices between the field isolation regions.

12. (Newly Added) The process of Claim 11, wherein growing the field oxide comprises exposing the field isolation regions to an oxidant consisting essentially of oxygen.

13. (Newly Added) The process of Claim 11, wherein growing the field oxide comprises exposing the field isolation regions at an oxidant partial pressure of less than about 30 atm.

Pub  
B4  
14. (Newly Added) A process of forming an integrated circuit on a semiconductor substrate, comprising:

masking portions of the substrate with a mask comprising silicon nitride;  
growing a field oxide by dry oxidation to a thickness sufficient for electrical isolation of devices within the substrate without forming silicon nitride inclusions therein;